CLAIMS

1. A process for manufacturing an integrated device, comprising:

forming integrated structures including semiconductor regions and isolation regions in a first wafer of semiconductor material;

forming interconnection structures of conductor material on a second wafer of semiconductor material, including forming plug elements each having a bonding region of a metal material capable of reacting with said semiconductor regions of said first wafer; and

bonding said first wafer and said second wafer together, including causing said bonding regions to react with said semiconductor regions.

2. The process according to claim 1, wherein said semiconductor material is silicon, and said step of causing said bonding region to react comprises forming a metal silicide.

3. The process according to claim 1, wherein said metal material is chosen from among titanium, nickel, platinum, palladium, tungsten, and cobalt.

4. The process according to claim 1, wherein said plug elements have a height, and said step of forming integrated structures comprises forming an insulating material layer on top of a substrate of semiconductor material, said insulating material layer having a thickness smaller than said height of said plug elements, and forming openings in said insulating material layer to uncover selective portions of said substrate (2), and wherein said step of bonding said first and second wafers comprises causing said bonding region to react with at least said selective portions of said substrate.

5. The process according to claim 1, wherein said step of forming integrated structures comprises forming an insulating material layer on top of a substrate of semiconductor material, and forming conductive regions (of semiconductor material on top of said insulating

material layer, and said step of bonding said first and second wafers comprises causing said bonding region to react with said conductive regions.

6. The process according to claim 1, wherein said step of forming interconnection structures comprises forming electrical connection regions of conductive material, and said step of forming plug elements comprises forming base regions of conductive material on top of and in direct electrical contact with said electrical connections regions, and forming said bonding regions on top of said base regions.

7. The process according to claim 1, wherein said step of forming integrated structures comprises forming integrated electronic components.

8. The process according to claim 1, wherein said step of forming integrated structures comprises forming micro-electromechanical systems.

9. The process according to claim 1, further comprising, before said step of bonding said first and second wafers, the step of forming self-alignment structures on said first and second wafers, and aligning said first and second wafers, using said self-alignment structures.

10. The process according to claim 9, wherein said step of forming self-alignment structures comprises forming at least one engagement seat in one of said first and second wafers, and forming at least one engagement element on another of said first and second wafers in a position facing said engagement seat.

11. The process according to claim 10, wherein said step of forming integrated structures comprises forming an insulating material layer on top of a substrate of semiconductor material, said step of forming at least one engagement seat comprises forming a guide opening in said insulating material layer, said guide opening having a basically trapezium shape, with a

major base and a minor base, and said engagement element having transverse dimensions smaller than said major base and greater than said minor base, and said step of aligning said first and second wafers comprises inserting said engagement element into said guide opening near said major base and displacing said second wafer with respect to said first wafer so to bring said engagement element towards said guide opening until said engagement element slots into said engagement seat.

12. The process according to claim 11, wherein said step of forming at least one engagement seat comprises forming a notch in said substrate beneath said guide opening, said step of forming an engagement element comprises forming at least one pin element of greater height than the thickness of said insulating material layer, and said step of displacing said second wafer comprises causing said pin element to snap into said notch before fittedly engaging said engagement element into said slotting seat.

13. An integrated device comprising:

a first body of semiconductor material housing integrated structures including semiconductor regions and isolation regions; and

a second body of semiconductor material carrying interconnection structures of conductive material wherein said interconnection structures include plug elements in direct contact with said semiconductor regions and have a bonding region of a material resulting from the reaction of said semiconductor regions with a metal material.

14. The device according to claim 13, wherein said semiconductor material is silicon, and said material resulting from the reaction of said semiconductor regions with a metal material is a metal silicide.

15. The device according to claim 13, wherein said metal material is chosen from among titanium, nickel, platinum, palladium, tungsten, and cobalt.

16. The device according to claim 13, wherein said plug elements have a height, said first body comprises an insulating material layer on top of a substrate of semiconductor material, said insulating material layer having a thickness smaller than the height of said plug elements, and openings uncovering selective portions of said substrate, and wherein said bonding region is bonded to said selective portions of said semiconductor regions.

17. The device according to claim 13, wherein said first body comprises an insulating material layer on top of a substrate of semiconductor material and conductive regions of semiconductor material on top of said insulating material layer, and wherein said bonding region is bonded to said conductive regions.

18. The device according claim 13, wherein said integrated structures comprise integrated electronic components.

19. The device according to claim 13, wherein said integrated structures comprise micro-electromechanical systems.

20. The device according to claim 13, wherein said first body and said second body comprise self-alignment structures.

21. The device according claim 20, wherein said self-alignment structures comprise at least one engagement seat (40) in one of said first and second bodies, and at least one engagement element on another of said first and second bodies in a position facing said engagement seat.

22. The device according claim 21, wherein said first body comprises a substrate of semiconductor material, an insulating material layer on top of said substrate, at least one guide opening in said insulating material layer, said guide opening having a basically trapezium shape, with a major base and a minor base, and said engagement element has

transverse dimensions smaller than said major base and greater than said minor base and extending in said guide opening in a position of interference with said engagement seat.

23. The device according claim 22, wherein said insulating material layer has a thickness, said substrate has a notch beneath said guide opening, and said engagement element comprises at least one pin element which has a greater height than the thickness of said insulating material layer and extends at least partially inside said notch.

24. A device comprising:

a first body of semiconductor material;

a second body of semiconductor material;

a plurality of plug elements formed on a surface of the second body; and

a plurality of bonding regions formed between the plug elements and a surface of the first body, the bonding regions being formed of a metal silicide resulting from a reaction of the semiconductor material of the first body with a metal material.

25. The device of claim 24, wherein the first and second semiconductor material bodies each comprise integrated structures, and wherein the plurality of plug elements provides electrical continuity between the integrated structures of the first body and the integrated structures of the second body.

26. The device of claim 24, wherein the first and second semiconductor material bodies comprise alignment means for positioning the bodies one with the other.

27. The device of claim 24, wherein the metal material is chosen from among titanium, nickel, platinum, palladium, tungsten, and cobalt.

28. The device of claim 24, wherein one of the plurality of plug elements has an annular shape, and encloses therein a region between the first and second semiconductor material bodies.

29. The device of claim 28, wherein a mechanical element is enclosed within the region between the first and second semiconductor material bodies and surrounded by the annular shaped plug element.

30. A process for manufacturing an integrated device, comprising:

forming integrated structures in a first wafer of semiconductor material, the first wafer including an exposed semiconductor region;

forming a bonding layer of a metal material on a second wafer of semiconductor material; and

bonding the first and second wafers together by causing the bonding layer to react with the semiconductor region.